

1/3

10
FOR (i=0; i<2; i=i+1)
11 { begin
out [i] = 8 ' b10101010;
enable [i] = up [2 * i];
end

Figure 1

reg y [3:0];
13 WHILE (x <= y)
12 begin
fpl_bit [x + y] - mm_iru [x - y];
end

Figure 2

16
18
20
14
22
FOR (INIT; EXIT; INC)
begin
BODY_OF_STATEMENTS;
end

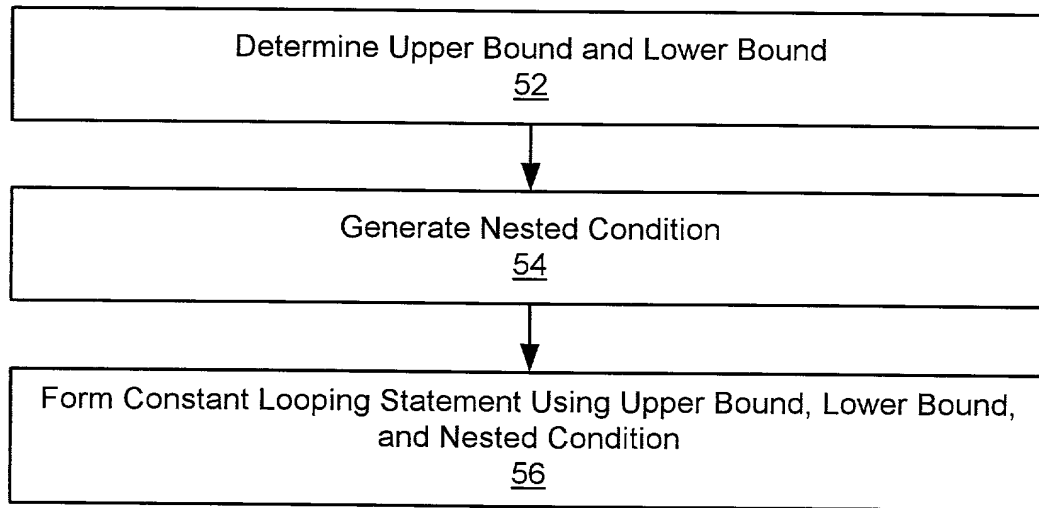
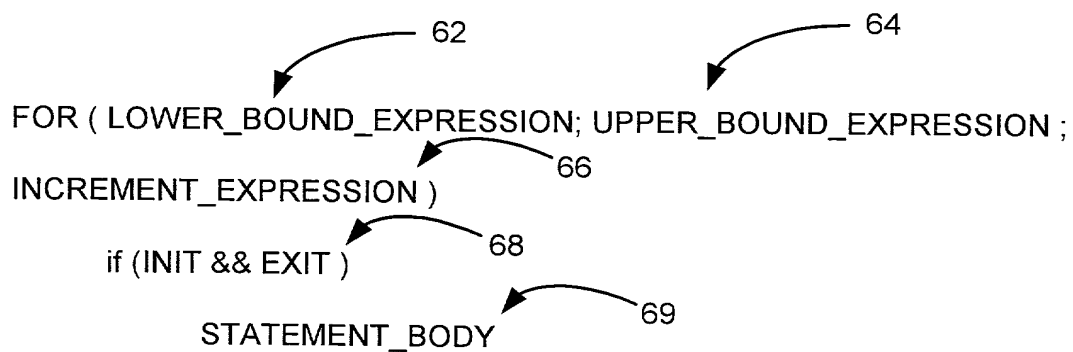
Figure 3

```

out [ 0 ] = 8 ' b10101010 ;
enable [ 0 ] = ~up [ 0 ] ;
}
out [ 0 ] = 8 ' b10101010 ;
enable [ 0 ] = ~up [ 2 ] ;
}

```

24

Figure 4**Figure 5****Figure 6**

80
 82 reg i [3 : 0] ;
 84 reg j [1 : 0] ;
 reg k [2 : 0] ; 74 76
 70 { for (j <= i ; i < k ; i = i + 1)
 statement_body 72 78

Figure 7

92 94 96
 90 { for (m = i ; m < 7 ; m + +)
 if (j <= m & & m < k)
 statement_body 98 100

Figure 8

110 { WHILE (x <= 15) 112
 if (x <= y)
 begin 114
 fpl_bit [x + y] = mm_iru [x - y] ; 116
 end

Figure 9